REMARKS

Claims 1-3, 5-26, 28, 29, and 31-39 are pending in the application. Claims 1-3, 5-26, 28, 29, and 31-39 stand rejected under 35 U.S.C. 102(e) and 35 U.S.C. 103(a) as allegedly being unpatentable in view of U.S. Patent No. 5,991,785 to Alidina et al. ("Alidina").

In view of the amendments and remarks herein, the rejections are respectfully traversed. Reconsideration and allowance are respectfully requested.

Claim 1

Claim 1 has been amended to include features of previous claim 3. As amended, claim 1 is patentable over Alidina because Alidina neither teaches nor suggests "pointer registers to store addresses of extreme data quantities in the array of N data elements," as recited in claim 1.

Instead, Alidina teaches that location information be determined in an entirely different way. In column 5, lines 35-44, Alidina explains that:

> The sign bits from adder 10 and the ALU are indicative of when the data value is more extreme than the corresponding running extremum. These sign bits are extracted as flags, which cause the transfer of the count of c1 (equal to the value of i) to registers ar1 and ar2, respectively. Thus, ar1 and ar2 store the count that existed when the corresponding running extremum occurred.

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14

This is related directly to the location of the running extremum in the data array, as will be discussed more fully below.

That is, Alidina does not use pointer registers pointing to an address of an extreme value in the array. Instead, Alidina tracks the counting variable "i," which is related to the relative position in the array which has the extreme value.

Since Alidina does not teach this feature of claim 1, claim 1 is patentable over Alidina.

Further, it would not have been obvious to modify Alidina to use pointer registers rather than storing the counting variable "i" to determine location information. There is no motivation to do so, since such a modification would change the principle of operation of Alidina (please see MPEP 2143.01) Rather than storing address information for the extreme values, Alidina stores information indicative of the relative position of the value within the array (the indicia "i"). Modifying Alidina to store address information using pointer registers would thus replace Alidina's technique with the different technique outlined in the current disclosure.

Claims 2, 3, and 5-10

Claims 2 and 5-10 depend from claim 1, and are therefore patentable for at least the same reasons as stated above with respect to claim 1.

15

Claim 3

Claim 3 is patentable for at least the additional reason that Alidina neither teaches nor suggests "further comprising determining an address of an extreme value based on a value in a pointer register and based on a correction factor to compensate for one or more errors," as recited in claim 3.

Examples of this feature are described in page 9 of the specification. As explained therein, errors may be introduced in the pipelining process. The values in the pointer registers may need to be corrected so that the location of the extreme values is correctly identified.

For at least this additional reason, claim 3 is patentable over Alidina.

Claim 11

Claim 11 includes features similar to those of claim 1, and is therefore patentable for at least similar reasons.

Claims 12, 36-39

Claims 12 and 36-39 depend from claim 11, and are patentable for at least the same reasons as stated above with respect to claim 11.

Claims 37 and 38

16

Claims 37 and 38 are further patentable because Alidina neither teaches nor suggests identifying a location of a last occurrence of a minimum or maximum in an array.

Alidina teaches identifying the location of a first occurrence of a minimum or maximum in an array. In Alidina, the counter is updated as the elements of the array are compared to the running extremum. When an element replaces the current running extremum, the value of the counter corresponding to that element is stored. At the end of the comparison, if the extreme value occurs more than once in the array, only the location of its first occurrence is determined.

In contrast, the current disclosure allows for determination of either the first or last occurrence of the extreme values, and allows a user to select which occurrence is determined (if desired). This provides an additional benefit that does not accrue using the systems and techniques of Alidina.

For at least this additional reason, claims 37 and 38 are patentable over Alidina.

Claim 13

Claim 13 includes features similar to those of claim 1 discussed above, and is therefore patentable for at least similar reasons.

17

Claims 14-18

Claims 14-18 depend from claim 13, and are thus patentable for at least the same reasons as stated above with respect to claim 13.

Claim 17

Claim 17 is patentable for at least the additional reason that Aladina neither teaches nor suggests "adjusting at least one of the pointer registers after processing all of the pairs of data elements to account for a number of stages in a pipeline."

The office action asserts that Alidina at column 5, lines 1-12 teaches this feature of claim 17. Alidina does not so teach. As explained above, Alidina does not use pointer registers at all. Instead, Alidina uses a counter to determine a local position of extreme values in the array.

Additionally, nowhere does Alidina adjust a register to account for a number of stages in a pipeline. The cited portion of Alidina instead teaches that the extreme values are determined from the values in the registers. No adjustment is made.

For at least this additional reason, claim 17 is patentable over Alidina.

Claim 19

18

Claim 19 includes features similar to those discussed above with respect to claim 1, and is therefore patentable for at least similar reasons.

Claims 20-25

Claims 20-25 depend from claim 19, and are therefore patentable for at least the same reasons as discussed above with respect to claim 19.

Claims 26 and 28

Claim 26 includes features similar to those of claim 1 discussed above, and is therefore patentable for at least similar reasons. Claim 28 depends from claim 26, and is therefore patentable for at least the same reasons.

Claim 29

Claim 29 includes features similar to those of claim 1 discussed above, and is therefore patentable for at least similar reasons.

Claims 31-35

Claims 31-35 depend from claim 29, and are therefore patentable for at least the same reasons.

19

CONCLUSION

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue, or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.
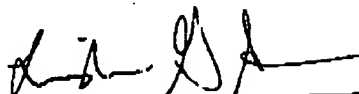
Claims 1-3, 5-26, 28, 29, and 31-39 are in condition for allowance, and a notice to that effect is respectfully solicited. If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-4311.

Attorney's Docket No.:10559/293001/P9300
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No fees are believed due. Please apply any charges or

credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date:_____11/15/04_____

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